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SYSTEM AND METHOD FOR EFFECTUATING THE TRANSFER OF DATA BLOCKS INCLUDING A HEADER BLOCK ACROSS A CLOCK BOUNDARY

PRIORITY UNDER 35 U.S.C. §119(e) & 37 C.F.R. §1.78

[0001] This nonprovisional application claims priority based upon the following prior United States provisional patent application entitled: "*System And Method For Effectuating The Transfer Of Data Blocks Including A Header Block Across A Clock Boundary*," Serial No.:60/469,504, filed May 10, 2003, in the names of Richard W. Adkisson and Huai-Ter Victor Chong, which is hereby incorporated by reference.

CROSS-REFERENCE TO RELATED APPLICATION(S)

[0002] This application discloses subject matter related to the subject matter disclosed in the following commonly owned co-pending patent application: "System and Method for Effectuating the Transfer of Data Blocks Across a Clock Boundary," filed _____, Docket No. 200300031-2, in the name(s) of: Richard W. Adkisson and Huai-Ter Victor Chong, which is hereby incorporated by reference.

BACKGROUND

[0003] By way of example, FIG. 1 depicts a timing sequence 100 of two clock domains having an N:(N-1) frequency ratio wherein data transfer across the clock boundary between the domains results in an extra data cycle or "dead cycle" in which data cannot be transferred. As is well known, data transfer operations between circuitry of a first clock domain and circuitry of a second clock domain are effectuated by synchronizer circuitry disposed therebetween. Further, the first and second clock domains are operable with clock signals that have a particular cycle ratio. For instance, the circuitry of the first clock domain ("fast clock domain") may be clocked with a first clock signal (CLK1) that is faster than a second clock signal (CLK2) used for clocking the circuitry of the second clock domain ("slow clock domain") such that there are N first clock cycles to (N-1) second clock cycles. In one application, core clock circuitry and bus clock circuitry of a computer system may represent the first and second clock domains, respectively, wherein CLK1 and CLK2 signals correspond to the core clock (CC) and bus clock (BC) signals.

[0004] A synchronizer controller circuit (not shown in FIG. 1) is usually provided for controlling the operation of synchronizer circuitry disposed between the two clock domains. Additionally, a control signal such as a SYNC pulse may be generated based on a predetermined temporal relationship between CLK1 and CLK2 for synchronizing the data transfer operations. For example, the SYNC pulse may be generated when a rising edge of the CLK1 signal coincides

with a rising edge of the CLK2 signal, which commences a data transmit window for the transfer of data blocks, which may include one or more data bits, from one clock domain to the other clock domain.

[0005] The timing sequence 100 of FIG. 1 illustrates an embodiment of CLK1 104, CLK2 106 and SYNC pulse signal 108, wherein for every five ticks of CLK1 there are four ticks of the slow clock (i.e., CLK2). A cycle count 102 refers to the numbering of CLK1 cycles in a particular data transmit window of the timing sequence 100. Data to be transferred from the fast clock domain is clocked at CLK1, that is, 5 data block pulses per window are available.

[0006] As alluded to before, the SYNC pulse 108 is high on coincident rising edges of CLK1 and CLK2 and the data transfer operations across the clock boundary between the two clock domains are timed with reference to the SYNC pulse. In a normal condition where there is no skew (or, jitter, as it is sometimes referred to) between CLK1 and CLK2, the coincident edges occur on the rising edges of the first cycle (cycle 0) as shown in FIG. 1. Since there are five CLK1 cycles and only four CLK2 cycles, CLK1 domain circuit portion cannot transmit data during one cycle resulting in what is known as a "dead tick," as CLK2 domain circuit portion does not have a corresponding time slot for receiving it. Typically, the cycle that is least skew tolerant is the one where data is not transmitted and, in the exemplary timing sequence shown in FIG. 1, it is the fourth cycle (i.e., cycle 3).

[0007] Skew between CLK1 and CLK2 signals can cause, for example, a variance in the positioning of the SYNC pulse which affects the data transfer operations between CLK1 and CLK2 domains. In the exemplary 5:4 frequency ratio scenario set forth above, if CLK2 leads CLK1 by a quarter cycle for instance, then instead of the edges being coincident at the start of cycle 0, they will be coincident at the start of cycle 1 and the dead tick's location may accordingly vary. In similar fashion, if CLK2 lags CLK1 by a quarter cycle, the edges will be coincident at the start of the last cycle (i.e., cycle 4). Regardless of the skew between the clock cycles, however, there will be a cycle where a data block cannot be sent, resulting in data transfer at less than full bandwidth. Furthermore, in channelized data transmission scenarios, where multiplexed data blocks are transmitted from a fast clock domain to a slow clock domain sequentially as contiguous data blocks, the latency introduced by dead cycles presents problems. Additionally, these problems can be particularly limiting where header blocks associated with multiplexed data blocks require excessive processing time.

SUMMARY

[0008] A system and method are disclosed that effectuate the transfer of data blocks including a header block across a clock boundary between a first clock domain and a second clock domain. In one embodiment, a first circuit portion provides the data blocks including the header block to a second circuit portion. Control logic associated with the second circuit portion is operable to process the header

block and generate in response to the header block a hint signal which is transferred via a synchronizer at least one data cycle prior to the transfer of the data blocks to a third circuit portion disposed in the second clock domain. A control block associated with the third circuit portion operates responsive to the hint signal to generate data transfer control signals for controlling the third circuit portion in order to control output of the data blocks in a particular ordered grouping.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] FIG. 1 (Prior Art) depicts a timing sequence of two clock domains having a known frequency ratio wherein data transfers across the clock boundary using a conventional synchronizer results in an extra data cycle in which data cannot be transferred;

[0010] FIG. 2 depicts a block diagram of a system for effectuating the transfer of data blocks including a header block across a clock boundary between a first clock domain and a second clock domain, wherein the header block is processed for generating an advance notification or "hint" of a data transfer operation;

[0011] FIG. 3 depicts a timing drawing of the various signals associated with the system for effectuating the transfer of data blocks including a header block;

[0012] FIG. 4 depicts a flow chart illustrating an embodiment of a method for effectuating the transfer of data blocks including a header block across a clock boundary between a first clock domain and a second clock domain;

[0013] FIG. 5A depicts a timing drawing of data received at a first cycle and sent data associated with a control signal of the system illustrated in FIG. 3;

[0014] FIG. 5B depicts a timing drawing of data received at a second cycle and sent data associated with the control signal of the system illustrated in FIG. 3;

[0015] FIG. 5C depicts a timing drawing of data received at a third cycle and sent data associated with the control signal of the system illustrated in FIG. 3;

[0016] FIG. 5D depicts a timing drawing of data received at a fourth cycle and sent data associated with the control signal of the system illustrated in FIG. 3; and

[0017] FIG. 5E depicts a timing drawing of data and received at a fifth cycle sent data associated with the control signal of the system illustrated in FIG. 3.

DETAILED DESCRIPTION OF THE DRAWINGS

[0018] In the drawings, like or similar elements are designated with identical reference numerals throughout the several views thereof, and the various elements depicted are not necessarily drawn to scale. Referring now to FIG. 2, therein is depicted a system 200 for effectuating the transfer of data blocks including a header block across a clock boundary between a first clock domain (e.g., a core clock domain) having N fast clock cycles and a second clock domain (e.g., a bus clock domain) having M slow clock cycles such that $N/M > 1$. Received data, e.g., core data generated by circuitry in the first clock domain, is provided on an incoming data path 202 at full bandwidth for transport to a

first circuit portion 204 that includes a channeled packet interface 206. The received data may include a data packet comprising N data pulses or blocks including a header block in a timing cycle window. The header block may provide protocol control information about the data packet and may be positioned at the beginning of a data packet, e.g., $H_0A_0B_0C_0D_0$.

[0019] In one embodiment, the data blocks are intervaled and each intervaled data block may include one or more bits that are spaced apart by an interval element which may include empty cycles. For example, the data may take the form $H_0\_A_0\_B_0\_C_0\_D_0$ wherein each "_" represents an empty cycle. In one embodiment, the received data may be multiplexed data that includes at least two sets of interleaved data blocks. In this embodiment, the data blocks are positioned in a spaced arrangement. For example, the data may take the form $H_0H_1A_0A_1B_0B_1C_0C_1D_0D_1$ if two packets of interleaved data blocks, i.e., data blocks $H_0A_0B_0C_0D_0$ and data blocks $H_1A_1B_1C_1D_1$, are present, or $H_0H_1H_2A_0A_1A_2B_0B_1B_2C_0C_1C_2D_0D_1D_2$ if three packets of interleaved data blocks, i.e., $H_0A_0B_0C_0D_0$, $H_1A_1B_1C_1D_1$ and $H_2A_2B_2C_2D_2$, are present. It should be appreciated, however, that the teachings presented herein are equally applicable to intervaled and non-intervaled data blocks.

[0020] The first circuit portion 204 provides the data blocks to a second circuit portion 208 via data path 210. Second circuit portion 208 includes at least one queue, for example, queues 214a through 214n, for transmitting data blocks to a multiplexer (MUX) block 216 via data paths 220a through 220n, respectively. In one embodiment, the queues are first-in-first-out (FIFO) queues. In order to transmit

the incoming intervaled data including a header block received via data path 210 as contiguous data, portions of the intervaled data are temporarily stored. The series of queues 214a through 214n provide temporary storage for the incoming data blocks received from the data path 210. The duration of the temporary storage, if required for a particular data block, depends on the total number of data blocks in the received data and the number of dead cycles. In one embodiment, the number of dead cycles equals N - M. Data path 218 transmits data received from the data path 210 to the MUX block 216 without queuing.

[0021] The header is stripped or removed from the incoming data packet and forwarded to a control logic block 222 associated with the second circuit portion 208. The control logic block 222 processes the header block and generates, in response to the header block, a hint signal 244 which is transferred at least one data cycle prior to the transfer of the data blocks to a third circuit portion 240 associated with the second clock domain. It should be appreciated that depending on the complexity of the data packet, the processing time of the header will vary. Accordingly, the transmission from the first clock domain and the receipt in the second clock domain of the data blocks contained in the data packet may be affected by the processing of the header.

[0022] To minimize the latency associated with header processing and solve associated timing issues, the control logic block 222 provides the third circuit portion 240 in the second clock domain with advance notice via the hint signal 244 which includes protocol control information relative to

the processing of the header block. This enables the third circuit portion 240 and other circuitry in the second clock domain time to prepare for the arrival of the data blocks. For example, depending on the processing time of the header, the data blocks associated with the header may need to be temporarily queued in the second clock domain or immediately forwarded to other circuitry in the second clock domain. Based on the information stored in the header and the number of dead cycles, the control logic block 222, which may take the form of a state machine, calculates the number of data blocks in the intervaled data and, accordingly, the length of time to store each data block and the appropriate location for the hint signal.

[0023] A synchronizer controller 224 is in communication with a core-to-bus synchronizer 226 as illustrated by a data flow line 228. The synchronizer controller 224 provides a series of dead cycle control signals, c2b_valid_ff 230 and c2b_valid_m_ff[4:1] 232, which provide zero to four cycles advance notice of the location or locations of the dead cycles between the first and second clocks. The synchronizer controller 224 provides its advance knowledge of the position of the dead cycles to the control logic block 222 so that the second circuit portion 208 may be controlled to send data to the synchronizer 226 whereby the sent data may be optimally arranged about the dead cycles, which dead cycles are to be removed by the synchronizer 226 in operation, resulting in an ordered and contiguous data output to the second clock domain. The control logic 222 associated with the second circuit portion provides a MUX selection control signal 234 to the MUX1 block 216 and a series of control signals

(control signals 238a-238n for clocking out data blocks stored in the queues 214a-214n) so that appropriate data blocks can be selected as MUX output.

[0024] Control block 242 (CLK2 domain) associated with the third circuit portion 240 operates responsive to the hint signal 244 transferred via the synchronizer 226 to generate a plurality of CLK2 domain control signals in order to anticipate the arrival of data and prepare the hardware of the second clock domain accordingly. One CLK2 domain control signal 246 may be registered using a control register 248 for generating a MUXSEL2 control signal 250 which controls a MUX2 252. The remaining CLK2 control signals 254a-254d control a SWAP block 256, a direct data path 258, a queue block 260, and a logic 0 block 262 so that the MUX2 252 can output the appropriate sequence of data blocks to an I/O data pad 264 via data path 266 in the second clock domain. Depending on the time taken by control logic block 222 to process the header, different control signals 254a-254d are employed. For example, if the processing of the header is delayed, then the control signal 254c may be sent to the queue 260 in order to buffer the transfer of the data from the synchronizer 226 into the second clock domain. Alternatively, if the processing of the header is occurring quickly, the control signal 254b and the data path 258 may be employed to forward the data directly to the I/O pad 264 of the second clock domain. Hence, the control block 242 operates responsive to the hint signal to generate data transfer control signals for controlling the third circuit portion in order to control output of the data blocks in a particular ordered grouping whether the ordered grouping involves temporarily storing the

data blocks or providing the data blocks to circuitry in the second clock domain without queuing.

[0025] Accordingly, the data blocks received from the channeled packet interface 206 are transmitted as contiguous data output with one or more interleaved dead cycles from the MUX1 block 216 to the synchronizer 226, i.e., a fast-to-slow synchronizer such as a core-to-bus synchronizer, operating under the control of the synchronizer controller 224. Additionally, as described, the hint signal is sent to circuitry in the second clock domain at least one cycle prior to the sending of the contiguous data output with one or more interleaved dead cycles. By way of illustration, continuing with the example of receiving multiplexed data, for instance, having two interleaved data packets including header blocks, such as $H_0H_1A_0A_1B_0B_1C_0C_1D_0D_1$, the data is transmitted sequentially and contiguously to a second clock domain third circuit portion 240 as $SA_0B_0C_0D_0A_1B_1C_1D_1$, wherein "S" is the hint signal. By providing the circuitry in the second clock domain with advance knowledge that a data block transfer may occur via a hint signal, the hardware of the second clock domain may make decisions in anticipation of the data blocks to move the data blocks into the second clock domain faster or slower, as required, thereby solving timing and throughput problems. Moreover, by interleaving the dead cycles between the first and second clocks, based on the advance knowledge provided by the synchronizer controller, into the contiguous data transmitted to the core-to-bus synchronizer, the present system minimizes latency and provides for the efficient transfer of data across clock boundaries.

[0026] FIG. 3 depicts a timing drawing of the various signals associated with the system 200 described hereinabove. As illustrated, the timing sequence 300 exemplifies an embodiment of a FIRST CLOCK 302, a SECOND CLOCK 304 and a SYNC pulse signal 306, wherein within each timing window, five FIRST CLOCK signals 302 are present for every four SECOND CLOCK signals 304. A cycle COUNT 308 refers to the numbering of FIRST CLOCK signals 302 in a particular data transmit window of the timing sequence 300. Received data 310, i.e., core data, includes two multiplexed data packets, packets 0 and 1 which are to be transferred from the fast clock domain as represented by the FIRST CLOCK signal 302 to the slow clock domain as represented by the SECOND CLOCK signal 304. The data blocks of each packet are designed by their respective subscripts 0 and 1. For example, packet 0 comprises data blocks A_0, B_0, C_0, and D_0 (with a header H_0) that are interleaved with the data blocks of packet 1 which include data blocks A_1, B_1, C_1, and D_1 (with a header H_1). The SYNC pulse signal 306 may be generated based on a predetermined temporal relationship between the FIRST CLOCK and the SECOND CLOCK. As illustrated, the SYNC pulse is high on the coincident rising edges of the FIRST CLOCK and the SECOND CLOCK and the data processing operations of the second circuit portion are timed with reference to the SYNC pulse. As alluded to in the Background, since the FIRST CLOCK has five cycles and the SECOND CLOCK has four cycles, the FIRST CLOCK domain circuit portion cannot transmit data during one cycle resulting in one dead cycle, as the SECOND CLOCK domain circuit portion does not have a corresponding time slot for receiving it. The dead cycle control signals, c2b_valid_ff

312, c2b_valid_m_ff[1] 314, c2b_valid_m_ff[2] 316, c2b_valid_m_ff[3] 318, and c2b_valid_m_ff[4] 320, provided by the synchronizer controller to the control logic are advance notice indicative of the location of the dead cycle between the FIRST CLOCK domain and the SECOND CLOCK domain. Specifically, the c2b_valid_ff control signal 312 indicates that the dead cycle is occurring at the 5th cycle, cycle 4, the c2b_valid_m_ff[1] control signal 314 provides one cycle advance notice that the dead cycle is at the 5th cycle, cycle 4, the c2b_valid_m_ff[2] control signal 316 provides two cycles advance notice that the dead cycle is at the 5th cycle, cycle 4, the c2b_valid_m_ff[3] control signal 318 provides three cycles advance notice that the dead cycle is at the 5th cycle, cycle 4, and the c2b_valid_m_ff[4] control signal 320 provides four cycles advance notice that the dead cycle is at the 5th cycle, cycle 4.

[0027] FIG. 4 depicts a flow chart of an embodiment of a method for effectuating the transfer of data blocks using a hint signal across a clock boundary between a first clock domain and a second clock domain. At block 400, a header block is processed in association with the data blocks that will be sent from the first clock domain to the second clock domain via a synchronizer. At block 402, a hint signal is generated responsive to the header block, which hint signal is positioned at least one cycle prior to the location of the data blocks. At block 404, the hint signal is transmitted to a control block in the second clock domain, thereby indicating that the data blocks may be sent to receiver circuitry in the second clock domain. At block 406, appropriate control signals are generated based on the hint

signal for controlling output of the data blocks in a particular ordered grouping.

[0028] FIG. 5A-5E depict a plurality of timing drawings of received data and sent data associated with a plurality of control signals described above. As illustrated in FIG. 3, with reference to the timing drawing 500 of FIG. 5A, five FIRST CLOCK signals 302 are present within each timing window for every four SECOND CLOCK signals 304. Also, a SYNC pulse 306 is present that affects the transfer operations between the FIRST CLOCK domain and the SECOND CLOCK domain. Since five FIRST CLOCK signals 302 are present for every four SECOND CLOCK signals 304, one dead cycle per transmission window is present. Multiplexed packets 0 and 1 provide interleaved data blocks, i.e., H_0, H_1, A_0, A_1, B_0, B_1, C_0, C_1, D_0, and D_1, or channeled packet data. In the timing drawing 500 of FIG. 5A, the synchronizer controller provides advance notice of the location of the dead cycle by sending control signal c2b_valid_ff 312 to the control logic. Control signal c2b_valid_ff 312 indicates that the fifth cycle, cycle 4, of the timing window is a dead cycle for the transmission of data from the fast clock domain to the slow clock domain. It should be appreciated that although FIGS. 5A-5E are described with relation to control signal c2b_valid_ff 312, the systems and methods of the present invention may be practiced with any of the aforementioned control signals 312-320. Accordingly, the control logic and MUX of the present system transmit sent data 502 including the hint signal contiguously, i.e., $SXA_0B_0C_0D_0XA_1B_1C_1D_1X$, optimally positioning the hint signal (S) and data blocks about the dead cycles (X). In the embodiment described, the hint signal prepares

the third circuit portion circuitry to forward the data blocks to receiving circuitry in the second clock domain without queuing. In particular, the positioning of the hint signal is adjusted so as not to coincide with a dead cycle. It should be appreciated that although timing drawing 500 only depicts packet 0 being transmitted (sent data 502), packet 1, i.e., $A_1B_1C_1D_1$, is transmitted as well. In particular, the following table illustrates the operations of one embodiment of the second circuit portion operating under control signal c2b_valid_ff 312 wherein data is received at the first cycle:

Table 1. Operation of Second Circuit Portion Under Control Signal c2b_valid_ff Upon Receiving Data at Cycle 0

CYCLE	OPERATION(S)
0	Receive header block H_0 at control logic
1	Receive header block H_1 at control logic
2	Receive data block A_0 from channeled packet interface (CPI) Temporarily store data block A_0 in a first queue
3	Receive data block A_1 from CPI Temporarily store data block A_1 in second queue Send hint signal generated responsive to header block H_0 Prepare third circuit portion to pass through data blocks without queuing
4	Receive data block B_0 from CPI Temporarily store data block B_0 in the first queue Receive zero cycle advance notice of the location of the dead cycle at cycle 4 No Transmission - Dead Cycle
0	Receive data block B_1 from CPI Temporarily store data block B_1 in the second queue Send data block A_0
1	Receive data block C_0 from CPI Temporarily store data block C_0 in the first queue Send data block B_0
2	Receive data block C_1 from CPI Temporarily store data block C_1 in the second queue Send data block C_0
3	Data block D_0 passes through via a register without queuing
4	Receive data block D_1 from CPI Temporarily store data block D_1 in the second queue Receive zero cycle advance notice of the location of the dead cycle at cycle 4 No Transmission - Dead Cycle
0	Send data block A_1
1	Send data block B_1
2	Send data block C_1
3	Send data block D_1
4	No Transmission - Dead Cycle

[0029] Similarly, FIGS. 5B-E depict various configurations of sent data having contiguous data blocks with a hint signal positioned relative to a dead cycle. For example, with reference to timing drawing 504 of FIG. 5B, the received data 310 is received at the second cycle and control signal c2b_valid_ff 312 indicates that the dead cycle is positioned at the fifth cycle, cycle 4. Accordingly, the sent data 506 including the hint signal is transmitted as $SA_0B_0C_0XD_0$. It should be appreciated that the dead cycle may appear to be interleaved in between two data blocks or at the leading end, i.e., before A_0, or at the trailing end, i.e., after D_0, of a data packet. By way of example, the dashed lines of data blocks A_0, B_0, C_0, and D_0 indicate that due to the processing of the header block H_0, the data blocks A_0, B_0, C_0 and D_0 were not transmitted/received between the clock domains. For example, the processing of header block H_0 is time-consuming and the data blocks A_0, B_0, C_0 and D_0 are temporarily queued in the second clock domain before being forwarded to circuitry in the second clock domain. The hint signal minimizes timing problems by providing advance knowledge to the second clock domain that the processing of the header is on-going. This allows the data blocks A_0, B_0, C_0, and D_0 to be temporarily stored in the second clock domain (i.e., CLK2) before being forwarded to the receive circuitry therein. The following table illustrates the operations of one embodiment of the second circuit portion operating under control signal c2b_valid_ff 312 during the first ten cycle counts wherein data is received at the second cycle:

Table 2. Operation of Second Circuit Portion Under Control Signal c2b_valid_ff Upon Receiving Data at Cycle 1

CYCLE	OPERATION(S)
1	Receive header block H_0 at control logic
2	Receive header block H_1 at control logic
3	Receive data block A_0 from CPI Temporarily store data block A_0 in a first queue
4	Receive data block A_1 from CPI Temporarily store data block A_1 in second queue Receive zero cycle advance notice of the location of the dead cycle at cycle 4
0	Receive data block B_0 from CPI Temporarily store data block B_0 in the first queue Send hint signal generated responsive to header block H_0 Prepare third circuit portion to queue the data blocks
1	Receive data block B_1 from CPI Temporarily store data block B_1 in the second queue Send data block A_0 Queue data block A_0 in CLK2 domain
2	Receive data block C_0 from CPI Temporarily store data block C_0 in the first queue Send data block B_0 Queue data block B_0 in CLK2 domain
3	Receive data block C_1 from CPI Temporarily store data block C_1 in the second queue Send data block C_0 Queue data block C_0 in CLK2 domain
4	Receive data block D_0 from CPI Temporarily store data block D_0 in the first queue Receive zero cycle advance notice of the location of the dead cycle at cycle 4 No Transmission - Dead Cycle
0	Receive data block D_1 from CPI Temporarily store data block D_1 in the second queue Send data block D_0 Queue data block D_0 in CLK2 domain

[0030] Similarly, with reference to timing drawing 508 of FIG. 5C, the received data 310 is received at the third cycle and the control signal c2b_valid_ff 312 indicates that the

dead cycle is positioned at the fifth cycle, cycle 4. Accordingly, sent data 510 including the hint signal is transmitted as $SA_0B_0C_0XD_0$ to the synchronizer. With reference to timing drawing 512 of FIG. 5D, the received data 310 is received at the fourth cycle and the control signal c2b_valid_ff 312 provides advance notice that the dead cycle is located at the fifth cycle, cycle 4. The circuit therefore transmits sent data 514 including the hint signal as $SA_0B_0XC_0D_0$. Similar to the sent data 506 of FIG. 5B, the data blocks A_0, B_0, C_0, and D_0 of sent data 514 are exemplified with dashed lines to indicate that the processing of the header is consuming additional cycles and the data blocks will be temporarily queued in the second clock domain before being forwarded to I/O receive circuitry therein. With reference to timing drawing 516 of FIG. 5E, the received data 310 is received at the fifth cycle and the control signal c2b_valid_ff 312 indicates that the dead cycle is located at the fifth cycle, cycle 4. Hence, sent data 518 including a hint signal is transmitted $SA_0XB_0C_0D_0$. Importantly, the control logic block sends the hint signal in a manner that accommodates the dead cycle. As illustrated by the variable arrival times of the received data 310 in FIGS. 5A-5E, the hint signal described herein provides notice of a possible data transfer regardless of the cycle at which data is received.

[0031] Accordingly, it should be appreciated that by practicing the teachings described herein, latency may be reduced during the transmission of received data which includes a header. In particular, during the processing of the header block in the first clock domain, a hint signal is

generated and positioned at least one cycle before the transmission of the data so that the hardware in the second clock domain can anticipate the arrival of the data and prepare accordingly. Moreover, it should be appreciated that the systems and methods described herein may be practiced with non-intervaled and any intervaled data, including multiplexed data, having any number of dead cycles.

[0032] Although the embodiments herein have been particularly described with reference to certain illustrations, it is to be understood that the forms of the invention shown and described are to be treated as exemplary embodiments only. Various changes, substitutions and modifications can be realized without departing from the spirit and scope of the invention as defined by the appended claims.